**Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

**Listing of Claims**

1. Claims 1-18 (Cancelled)

19. (Currently Amended) An apparatus comprising:

a first printed circuit board;

a processor mounted to the first printed circuit board, wherein the processor comprises a development port and a memory controller~~, wherein the development port comprises a full duplex serial interface~~;

a system bus formed on the first printed circuit board and coupled to the ~~processor~~ memory controller;

a second bus formed on the first printed circuit board and coupled to the development port;

a random access memory mounted on the first printed circuit board and coupled to the memory controller via the system bus, wherein the random access memory stores a copy of an operating system;

wherein the development port is configured to transfer configuration information to the memory controller;

wherein the memory controller is configured to read some or all of the operating system copy stored in the random access memory via the system bus after the memory controller receives the configuration information via the development port.

20. (Currently Amended) The apparatus of claim 19 further comprising

a second printed circuit board;

a first data storage device mounted on the second printed circuit board, wherein the first data storage device stores ~~boot-up-code~~ the configuration information;

a coupler, coupling the first printed circuit board to the second printed circuit board, defining at least a first data communication path from said second printed circuit board to said first printed circuit board;

wherein the ~~boot-up-code~~ the configuration information can be transmitted from the first storage device, over the first communication path, said second bus, to said development port of the processor.

21. (Previously Presented) The apparatus of claim 20 wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.

22. (Currently Amended) The apparatus of claim 20 wherein ~~the second printed circuit board is configured to download the boot-up-code to~~ the development port is configured to transfer the configuration information automatically, in response to a power up or a reset of the apparatus.

23. (Cancelled) The apparatus of claim ~~20 wherein the first printed circuit board comprises a DRAM coupled to a memory controller and wherein said boot-up-code comprises configuration information for configuring the memory controller~~ 22 wherein the memory controller is configured to read some or all of the operating system copy stored in the random access memory after the memory controller receives the configuration information and in response to the power up or the reset of the apparatus.

24. (Currently Amended) The apparatus of claim 23 ~~wherein the DRAM is coupled to the system bus~~ wherein the development port comprises a full duplex serial interface.

25. (Previously Presented) The apparatus of claim 19 wherein the second bus comprises a serial data bus.

26. (Currently Amended) A method of booting up a system, wherein the system comprises a motherboard coupled to daughterboard, wherein the daughterboard comprises a microprocessor, a system bus, a random access memory that stores a copy of an operating system, and a second bus, ~~wherein the microprocessor is coupled to the system bus and the second bus,~~ wherein the microprocessor comprises a development port coupled to the second bus, wherein the microprocessor comprises a memory controller, wherein the memory controller is coupled to the random access memory via the system bus, the method comprising:

transmitting ~~a first boot-up code~~ memory controller configuration information from said motherboard to said memory controller via the development port ~~via~~ and the second bus, in response to a power-on or reset of said system~~, wherein the development port comprises a full duplex serial interface~~; and

~~using said boot-up code, in said microprocessor to perform a first boot-up operation~~ the memory controller reading some or all of the operating system copy stored in the random access memory via the system bus after the memory controller receives the memory controller configuration information via the development port and in response to the power-on or reset of said system.

27. (Currently Amended) The method of claim 26 ~~wherein said boot-up operation comprises configuring a port of the microprocessor that is different from said development port~~ transmitting the copy of the operating system from the motherboard to the random access memory for storage therein.

28. (Currently Amended) The method of claim 26 ~~wherein said daughterboard comprises a DRAM and a memory controller, and wherein said boot-up operation comprises configuring said memory controller~~ wherein the development port comprises a full duplex serial interface.

29. (Currently Amended) The method of claim 26 ~~wherein said daughterboard comprises a DRAM coupled to the system bus, and wherein the method further comprises transmitting data from the mother board to the DRAM via the system bus~~ further comprising transmitting the operating system copy from the motherboard to the random access memory for storage therein via the development port, after the memory controller receives the memory controller configuration information via the development port and in response to the power-on or reset of said system.

30. (Currently Amended) The method of claim 29 wherein the ~~data comprises an operating system for said microprocessor~~ memory controller configuration information is transferred to the memory controller from a memory device on said motherboard.

31. (Currently Amended) An apparatus comprising:

a first printed circuit board coupled to a second printed circuit board;

a processor mounted to the first printed circuit board, wherein the processor comprises a development port and a memory controller~~, wherein the development port comprises a full duplex serial interface~~;

a random access memory mounted on the first printed circuit board and configured to store a copy of an operating system;

a system bus formed on the first printed circuit board and coupled ~~to the processor~~ to the random access memory and the memory controller;

a second bus coupled to the development port, wherein the second bus is formed on the first printed circuit board;

means for downloading ~~a boot up code~~ memory controller configuration information from said second printed circuit board to said memory controller via the development port ~~via~~ and the second bus, in response to a power on or reset of said apparatus.

32. (Previously Presented) The apparatus of claim 31 wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.